IN THE CLAIMS:

1 (currently amended). A semiconductor device comprising:

at least one memory cell configured to generate a first voltage on a first bit line and including a switching device having a first resistance;

at least one reference cell configured to generate a second voltage on a second bit line and including:

a first resistive element coupled between a voltage source and the second bit line and having a second resistance; and

a second resistive element coupled between a sink and the second bit line and having a third resistance; and

a sense amplifier for generating an output in response to the first and the second voltages;

wherein the memory cell comprises a NDR and an access device.

Claims 2-4 (cancelled).

5 (currently amended). The semiconductor of claim 1 [[4]] wherein the NDR comprises a thyristor.